AMENDMENTS TO THE SPECIFICATION

On page 3, please delete the last full paragraph and replace it with the following new paragraph:

As shown in FIG. 17A, 17B, it [[is]] has been found that the threshold voltage values reflect no change ~~indicates no changes~~ between the values measured before and after the application of the bias voltage, whereas the drain current decreases. ~~That is, it is thought that~~ These results indicate the main factor ~~of decreasing of the~~ resulting in the decreased drain current ~~does not depend on a decreasing of the~~ is not decreased threshold voltage, but ~~depends on the~~ rather other unknown factors.

On page 8, please delete the second full paragraph and replace it with the following new paragraph:

A gate electrode 29 made of polysilicon is formed on the channel forming region 24a of the channel well layer 24 with a gate oxide film 30 interposed therebetween. This gate electrode 29 is formed in a manner that a part of it overlaps onto the LOGOS oxide film 28, that is. a part of it is protruded onto the LOGOS oxide ~~films~~ film 28. In this case, a protrusion amount (hereinafter, called "gate overlap length"[[:]] shown as O/L in FIG. 1) of the gate electrode 29 onto the LOGOS oxide film 28 is set to substantially 10 μm, which is 1/2 (a half) of the width size W of the LOGOS oxide film 28.

On page 8 and 9, please delete the bridging paragraph and replace it with the following new paragraph:

An interlayer insulating film 33 made of ~~such as~~ a silicon oxide film is formed so as to cover the LOGOS oxide film 28 and gate electrode 29 and so on. Furthermore, a final passivation film 34 is formed so as to cover the interlayer insulating film 33, the drain electrode 31, and the source electrode 32.

On page 9, please delete the third full paragraph and replace it with the following new paragraph:

In this case of the LDMOS 21 structured as [[the]] described above, it is found that the following ~~phenomenons~~ phenomena (1) to (3) occur when a bias is applied so as to maintain the LDMOS 21 with OFF condition.

On page 9 and 10, please delete the bridging paragraph and replace it with the following new paragraph:

(3) As shown in FIG. SA-5B, [[a]] the hot carrier flow in the neighborhood of the surface of the monocrystal silicon substrate 22 (especially, in the neighborhood of surface corresponding to the LOGOS oxide film 28 and a lower region of the drain-contact layer 27) contains a vertically negative component (in a direction away from the LOGOS oxide film 28 and into the monocrystal silicon substrate 22) ~~toward lower side~~

~~(the opposite side direction of the LOGOS oxide film 28)~~ below the LOGOS oxide film 28.

On page 11, please delete the second full paragraph and replace it with the following new paragraph:

According to FIG. 3, when the O/L is set to 5 μm and 7 μm (the samples that the current change rate during the application of the bias voltage indicates negative value), the peak (maximum electric field point) of the electric field intensity distribution described [[the]] above is shifted from the central portion of the LOGOS oxide film 28 to the source diffusion layer 25 side. However, when the O/L is set to 10 μm (the samples that the current change rate during the application of the bias voltage indicates positive value), the maximum electric ~~filed~~ field point in the neighborhood of the surface of the monocrystal silicon substrate 22 occurs at a substantially central portion of a region corresponding to the LOGOS oxide film 28.